Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **1 OUT**
2. **1 IN-**
3. **1 IN+**
4. **Vcc-**
5. **2 IN+**
6. **2 IN-**
7. **2 OUT**
8. **Vcc+**

**.074”**

**.076”**

**1 8 7**

**2**

**3**

**6**

**5**

**4**

**TLE**

**2062B**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0036” X .0036”**

**Backside Potential: Vcc- (or leave FLOATING)**

**Mask Ref: TLE 2062B**

**APPROVED BY: DK DIE SIZE .074” X .076” DATE: 4/27/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .015” P/N: TLE2062**

**DG 10.1.2**

#### Rev B, 7/19/02